REMARKS/ARGUMENTS

The Office Action mailed March 27, 2003 has been received and carefully considered. Claims 1- 18 are pending in the application, claims 13-18 being newly presented.

Claims 1 - 12 stand rejected under 35 U.S.C. § 103 (a) as being unpatentable over Spivey et al. (U.S. Patent No. 5,886,353, hereinafter "Spivey") in view of Sayag et al. (U.S. Patent No. 5,510,623, hereinafter "Sayag") in further view of Thevenin et al. (U.S. Patent No. 5,937,027, hereinafter "Thevenin") in still further view of Heller et al. (U.S. Patent No. 6,396,539, hereinafter "Heller"). These rejections are respectfully traversed.

Heller is not addressed herein in response to the rejections above because Heller was filed February 27, 1998 while the present application claims priority from a provisional application filed December 16, 1997. Heller, therefore, cannot be considered prior art to the present application.

Generally speaking, the present invention is directed towards image sensors that have row logic inside an image sensor and have chip drivers and pixel interpolator along a fourth edge of the image sensor. The invention is also generally directed to an image sensor circuit formed from at least two image sensors that are butted to each other. Each of the image sensors has chip driver circuitry and pixel interpolation circuitry.

Thus, the invention as defined in Claim 1 is as follows:

> A CMOS image sensor circuit, comprising:
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> a first CMOS image sensor substrate, said substrate having an image sensor portion arranged in an array of pixels of rows and columns, and image sensor logic on said substrate, said image sensor logic being electrically connected to said image sensor portion, said image sensor logic including row logic associated with

each of said rows individually, and chip logic associated with parts of said image sensor portion other than said rows individually, said image sensor portion having a first portion and a second portion;

said image sensor substrate formed to have at least a first set of parallel edges including a first edge and a second edge, and a second set of parallel edges, different than said first set of parallel edges, and second set of parallel edges including a third edge and a fourth edge;

said image sensor substrate extending between said first edge, said second edge, and said third edge, such that said first portion of said image sensor portion is adjacent said first edge and said third edge of said image sensor substrate and said second portion of said image sensor portion is adjacent said second edge and said third edge of said image sensor substrate;

said row logic being physically located inside said image sensor in place of a plurality of pixels of the array forming said image sensor;

a pixel interpolator and said chip driver circuitry located between said first portion and said second portions of said image sensor portion and said fourth edge of said image sensor substrate; and

a second CMOS image sensor substrate configured similarly to said first CMOS image sensor substrate and abutted to one of said edges of said first CMOS image sensor substrate.

Spivey describes a pixel array for an x-ray image sensor including pixel circuits 11 disposed in the interior of a chip (see FIGs. 3 and 4). Spivey's readout circuit 18, including shift registers 32, 36, sample-and-hold circuitry 54 and wire bond pads, is disposed at the edges of the chip. The 128 pixel circuits are all visible on FIG. 3 as 8 rows of 16 circuits. See col. 5, line 57 to col. 5, line 1 and FIGs. 3 and 4.

The pixel array and readout circuitry is carried on chip carrier 153 to which is attached is a connector 184 for attaching a ribbon cable 167. The connector 184 and ribbon cable 167 are disposed on an underside of the chip carrier. See col. 11, line 57 to col. 12, line 5 and col. 13, line 4 – 28 and FIGs. 15A and 15B.

Spivey further describes an image sensor formed of a plurality of the image sensors wherein a first column of the image sensors are butted on each of two sides with gaps 186

between the butted joints both in the row and column direction. A second column is also formed which is attached beneath the first column in a shingle fashion. Additional gaps occur between the columns 189. The gaps 186, 189 are non-responsive to x-rays (images). See col. 13, line 45 to col. 14, line 8 and FIGs. 17A and 17B.

Spivey further describes an image sensor for use with fluoroscopy having a pixel array with integrated readout circuitry. The large format fluoroscopy image sensor is possible because the pixel circuitry in each pixel occupies only about 15% of the pixel area and where "Wire bond connections are made to select pixel locations at the periphery of the array. These pixel locations are treated as dead pixels." See Col. 26, lines 43 – 46.

Spivey does not have "row logic being physically located inside said image sensor in place of a plurality of pixels of the array forming said image sensor" as recited in claim 1, but rather the row logic is disposed at the periphery of the image sensor and not in place of a plurality of pixels. In further contrast to the present invention, Spivey does not have "said image sensor substrate extending between said first edge, said second edge, and said third edge, such that said first portion of said image sensor portion is adjacent said first edge and said third edge of said image sensor substrate and said second portion of said image sensor portion is adjacent said second edge and said third edge of said image sensor substrate" as recited in claim 1. In still further contrast to the present invention, Spivey does not describe "a pixel interpolator" as recited in claim 1, but rather treats the pixel locations as dead pixels.

Thevenin describes an image sensor having two types of pixels, image pixels 10 and measurement or dose pixels 11. Beneath each zone having image pixels are reading circuits 12a, 12b, 12c and 12d. There are two rows of measurement pixels in the row and column

direction to form a cross between the reading circuits. The charges received from the measurement pixels are transferred to the neighboring pixels (image pixels). That is, the image sensor described by Thevenin does not have "row logic being physically located inside said image sensor in place of a plurality of pixels of the array forming said image sensor" as recited in claim 1, but rather has measurement pixels that are disposed between the zones of image pixels. See col. 6, line 47 – col. 7, line 5 and col. 7, line 22 – 26 and FIG. 3A and 3B. Thevenin does not teach buttable image sensors. That is, Thevenin does not have "a second CMOS image sensor substrate configured similarly to said first CMOS image sensor substrate and abutted to one of said edges of said first CMOS image sensor substrate". Thevenin also fails to describe the recited "pixel interpolator".

Sayag describes a CCD image sensor array having a centrally disposed photosensitive readout register thus creating a CCD image sensor having two halves. At col. 3 lines 6, - 15, Sayag specifies chamfered corners for the image sensor avoiding the use of an "amplifier corner". The image sensor of Sayag has chamfered corners. Sayag's image sensors are not butted as recited in Claim 1 nor are they buttable without substantial image loss at the corners of the image sensor. Further, Sayag corrects for image loss at the photosensitive readout register area by multiplying the pixels of the photosensitive readout register area by a constant to match the other pixels (see col. 7, lines 6 – 8). In further contrast to the present invention, Sayag does not have "a pixel interpolator".

Accordingly, the references, even when considered in combination, do not teach or suggest the claimed invention. Specifically, none of the references cited teach or suggest a pixel interpolator. Moreover, Spivey does not have row logic inside the image sensor in place of a plurality of pixels and teaches away from the use of a pixel interpolator by

treating the pixel locations taken by the wire bond connections as dead pixels, Thevenin does not teach buttable image sensors and Sayag teaches away from the idea of butting a plurality of image sensors with the description of the chamfered corners. Because of these disparate teachings, there is no motivation to combine references in any logical fashion, except as a hindsight reconstruction of the invention. Neither Spivey nor Thevenin teach row logic inside an image sensor in place of a plurality of pixels. Spivey teaches away from using a pixel interpolator instead treating the pixels as dead pixels; Sayag teaches away from pixel interpolation opting instead for multiplication by a constant; Thevenin teaches away from pixel interpolation by transferring the measurement pixel charge to neighboring image pixels. Thus, not only do none of Spivey, Thevenin and Sayag teach each and every feature of the invention as recited in Claim 1, there is no logical rational or motivation for combining them together.

It is, therefore, respectfully submitted that Claim 1 is patentable over the art of record for at least the above reasons. Claims 2 – 7 depend directly or indirectly from Claim 1 so are also respectfully submitted to be patentable over the art of record.

Independent claim 8 stands rejected based on the references and rejections of claims 1 and 3. Claim 8 recites:

> A method of operating a large format image sensor, comprising:
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> first obtaining an image sensor chip which has first and second edges where said image sensor comes within two pixel pitches of said first and second edges, and includes row selecting logic in place of a plurality of central pixels of the image sensor;
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> abutting said image sensor chip against a similar image sensor chip of corresponding construction; and
>
> interpolating missing pixels caused by both said row select logic and by

spaces between said image sensor chips.

None of the references cited teach pixel interpolation. Moreover, Spivey does not have row logic inside the image sensor in place of a plurality of pixels and teaches away from the use of a pixel interpolator by treating the pixel locations taken by the wire bond connections as dead pixels. Thevenin does not teach buttable image sensors, and Sayag teaches away from the idea of butting a plurality of image sensors with the description of the chamfered corners. Because of these disparate teachings, there is no motivation to combine references in any logical fashion, except as a hindsight reconstruction of the invention. Neither Spivey nor Thevenin teach row logic inside an image sensor in place of a plurality of pixels. Spivey teaches away from using a pixel interpolator instead treating the pixels as dead pixels; Sayag teaches away from pixel interpolation opting instead for multiplication by a constant; Thevenin teaches away from pixel interpolation by transferring the measurement pixel charge to neighboring image pixels. Thus, not only do the references not teach each and every feature of the invention as recited in Claim 8, there is also no logical rational or motivation for combining them together.

It is, therefore, respectfully submitted that Claim 8 is patentable over the art of record for at least the above reasons.

Independent claim 9 stands rejected based on the references and rejections of claim 1. Claim 9 recites:

> A CMOS imager, comprising:
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> a first CMOS image sensor having an image sensor portion arranged in an array of rows and columns, said first CMOS image sensor formed to have at least a first set of parallel edges including a first edge and a second edge, and a

second set of parallel edges, different than said first set of parallel edges, and second set of parallel edges including a third edge and a fourth edge;

said first CMOS image sensor having a control portion and a centralized row-local control portion, said centralized row-local control portion being physically located inside said image sensor in place of a plurality of pixels of the array forming said image sensor thereby forming at least two image sensor areas; and

said control portion including a pixel interpolator located between said at least two image sensor areas and one of said edges of said image sensor.

None of the references cited teach a pixel interpolator. Moreover, Spivey does not have row logic inside the image sensor in place of a plurality of pixels and teaches away from the use of a pixel interpolator by treating the pixel locations taken by the wire bond connections as dead pixels. Neither Spivey nor Thevenin teach row logic inside an image sensor in place of a plurality of pixels. Because of these disparate teachings, there is no motivation to combine references in any logical fashion, except as a hindsight reconstruction of the invention. Spivey teaches away from using a pixel interpolator instead treating the pixels as dead pixels; Sayag teaches away from pixel interpolation opting instead for multiplication by a constant; Thevenin teaches away from pixel interpolation by transferring the measurement pixel charge to neighboring image pixels. Thus, not only do the cited references not teach each and every feature of the invention as recited in Claim 9, there is also no logical rational or motivation for combining them together.

It is, therefore, respectfully submitted that Claim 9 is patentable over the art of record for at least the above reasons. Claim 10 depends directly from Claim 9 so is also respectfully submitted to be patentable over the art of record.

Independent claim 11 stands rejected based on the references and rejections of claim 1. Claim 11 recites:

A method of fabricating a CMOS imager comprising:

fabricating at least two CMOS image sensors having an image sensor portion arranged in an array of rows and columns, said at least two CMOS image sensors formed to have at least a first set of parallel edges including a first edge and a second edge, and a second set of parallel edges, different than said first set of parallel edges, and second set of parallel edges including a third edge and a fourth edge, said at least two image sensor having a control portion and a centralized row-local control portion, said centralized row-local control portion being physically located inside said image sensor in place of a plurality of pixels of the array forming said image sensor thereby forming at least two image sensor areas, said control portion including a pixel interpolator located between said at least two image sensor area and one of said edges of said image sensor;

abutting said at least two CMOS image sensors together; and

integrating said control portions of said at least two CMOS image sensors such that said at least two CMOS image sensors function as a single CMOS imager.

None of the references cited teach pixel interpolation. Moreover, Spivey does not have row logic inside the image sensor in place of a plurality of pixels and teaches away from the use of a pixel interpolator by treating the pixel locations taken by the wire bond connections as dead pixels, Thevenin does not teach abutting image sensors together and Sayag teaches away from the idea of butting a plurality of image sensors with the description of the chamfered corners. Because of these disparate teachings, there is no motivation to combine references in any logical fashion, except as a hindsight reconstruction of the invention. Neither Spivey nor Thevenin teach row logic inside an image sensor in place of a plurality of pixels. Spivey teaches away from using a pixel interpolator instead treating the pixels as dead pixels; Sayag teaches away from pixel interpolation opting instead for multiplication by a constant; Thevenin teaches away from pixel interpolation by transferring the measurement pixel charge to neighboring image pixels. Thus, not only do none of the

cited references not teach each and every feature of the invention as recited in Claim 11, there is also no logical rational or motivation for combining them together.

It is, therefore, respectfully submitted that Claim 11 is patentable over the art of record for at least the above reasons. Claim 12 depends directly from Claim 11 so is also respectfully submitted to be patentable over the art of record.

Newly presented independent claims 13, 15 and 17 are similarly respectfully submitted to be patentable over the art of record for at least the above reasons. Claim 14 depends directly from claim 13 so is also respectfully submitted to be patentable over the art of record. Claim 16 depends directly from claim 15 so is also respectfully submitted to be patentable over the art of record. Claim 18 depends directly from claim 17 so is also respectfully submitted to be patentable over the art of record.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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